20 µA Maximum, Rail-to-Rail I/O, Zero Input Crossover Distortion Amplifiers

AD8506

FEATURES

PSRR: 100 dB minimum
CMRR: 105 dB typical
Very low supply current: 20 µA per amp maximum
1.8 V to 5.5 V single-supply operation
Rail-to-rail input and output
Low noise
  2.8 µV p-p from 0.1 Hz to 10 Hz
  45 nV/√Hz @ 1 kHz
2.5 mV offset voltage maximum
Very low input bias current: 1 pA typical

APPLICATIONS

Pressure and position sensors
Remote security
Bio sensors
IR thermometers
Battery-powered consumer equipment
Hazard detectors

PIN CONFIGURATION

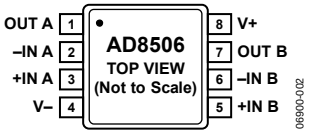

Figure 1. 8-Lead MSOP (RM Suffix)

GENERAL DESCRIPTION

The AD8506 is a dual micropower amplifier featuring rail-to-rail input and output swings while operating from a 1.8 V to 5.5 V single power supply.

Using a novel circuit technology, these low cost amplifiers offer zero crossover distortion (excellent PSRR and CMRR performance) and very low bias current, while operating with a supply current of less than 20 µA per amplifier. This amplifier offers the lowest noise in its power class.

This combination of features makes the AD8506 amplifier an ideal choice for battery-powered applications because it minimizes errors due to power supply voltage variations over the lifetime of the battery and maintains high CMRR even for a rail-to-rail input op amp.

Remote battery-powered sensors, handheld instrumentation and consumer equipment, hazard detection (for example, smoke, fire, and gas), and patient monitors can benefit from the features of the AD8506 amplifier.

The AD8506 is specified for both the industrial temperature range of −40°C to +85°C and the extended industrial temperature range of −40°C to +125°C. AD8506 dual amplifiers are available in 8-lead MSOP packages.

Rev. 0

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REVISION HISTORY

11/07—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{SY} = 5 V, V_{CM} = V_{SY}/2, T_A = 25°C, R_L = 100 kΩ to GND, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	0 V < V_{CM} < 5 V		0.5	2.5	mV
		−40°C < T_A < +125°C			3	mV
Input Bias Current	I_B			1	10	pA
		−40°C < T_A < +85°C			100	pA
		−40°C < T_A < +125°C			600	pA
Input Offset Current	I_{OS}			0.5	5	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			130	pA
Input Voltage Range		−40°C < T_A < +125°C	0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	90	105		dB
		−40°C < T_A < +85°C	90			dB
		−40°C < T_A < +125°C	85			dB
Large Signal Voltage Gain	A_{VO}	0.05 V < V_{OUT} < 4.95 V	105	120		dB
		−40°C < T_A < +125°C	100			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		2		µV/°C
Input Capacitance	C_{DIFF}			3		pF
	C_{CM}			4.2		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	4.98	4.99		V
		−40°C < T_A < +125°C	4.98			V
		R_L = 10 kΩ to GND	4.9	4.95		V
		−40°C < T_A < +125°C	4.9			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_S		2	5	mV
		−40°C < T_A < +125°C			5	mV
		R_L = 10 kΩ to V_S		10	25	mV
		−40°C < T_A < +125°C			25	mV
Short-Circuit Limit	I_{SC}			±55		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 1.8 V to 5 V	100	110		dB
		−40°C < T_A < +85°C	100			dB
		−40°C < T_A < +125°C	95			dB
Supply Current/Amplifier	I_{SY}	V_O = V_S/2		15	20	µA
		−40°C < T_A < +125°C			25	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 10 pF, A_V = +1		13		mV/µs
Gain Bandwidth Product	GBP			100		kHz
−3 dB Bandwidth				150		kHz
Phase Margin	Φ_M			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_{n\,p\text{-}p}$	f = 0.1 Hz to 10 Hz		2.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		80		fA/√Hz

V_{SY} = 1.8 V, V_{CM} = V_{SY}/2, T_A = 25°C, R_L = 100 kΩ to GND, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	0 V < V_{CM} < 1.8 V		0.5	2.5	mV
		−40°C < T_A < +125°C			3	mV
Input Bias Current	I_B			1	10	pA
		−40°C < T_A < +85°C			100	pA
		−40°C < T_A < +125°C			600	pA
Input Offset Current	I_{OS}			0.5	5	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			100	pA
Input Voltage Range		−40°C < T_A < +125°C	0		1.8	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1.8 V	85	100		dB
		−40°C < T_A < +85°C	85			dB
		−40°C < T_A < +125°C	80			dB
Large Signal Voltage Gain	A_{VO}	0.05V < V_{OUT} < 1.75V	95	115		dB
		−40°C < T_A < +125°C	95			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		2.5		µV/°C
Input Capacitance	C_{DIFF}			3		pF
	C_{CM}			4.2		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	1.78	1.79		V
		−40°C < T_A < +125°C	1.78			V
		R_L = 10 kΩ to GND	1.65	1.75		V
		−40°C < T_A < +125°C	1.65			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_S		2	5	mV
		−40°C < T_A < +125°C			5	mV
		R_L = 10 kΩ to V_S		12	25	mV
		−40°C < T_A < +125°C			25	mV
Short-Circuit Limit	I_{SC}			±6.5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 1.8 V to 5 V	100	110		dB
		−40°C < T_A < +85°C	100			dB
		−40°C < T_A < +125°C	95			dB
Supply Current/Amplifier	I_{SY}	V_O = V_S/2		16.5	20	µA
		−40°C < T_A < +125°C			25	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 10 pF, A_V = +1		13		mV/µs
Gain Bandwidth Product	GBP			100		kHz
−3 dB Bandwidth				150		kHz
Phase Margin	Φ_M			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_{n\ p\text{-}p}$	f = 0.1 Hz to 10 Hz		2.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
Current Noise Density	i_n	f = 1 KHz		80		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	5.5 V
Input Voltage	$\pm V_{SY}$
Differential Input Voltage[1]	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Differential input voltage is limited to 5.5 V or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM)	190	44	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

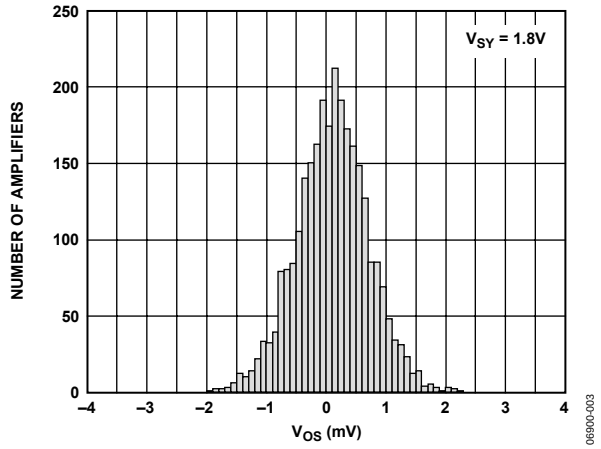


Figure 2. Input Offset Voltage Distribution

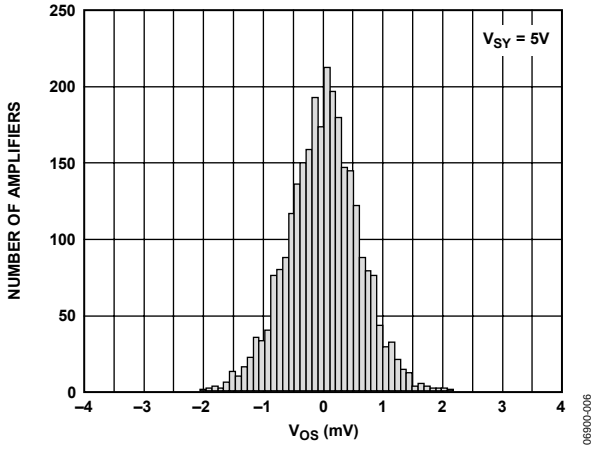


Figure 5. Input Offset Voltage Distribution

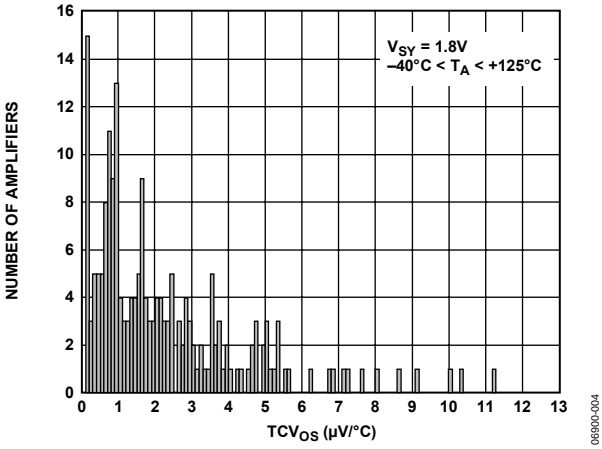


Figure 3. Offset Voltage Drift Distribution

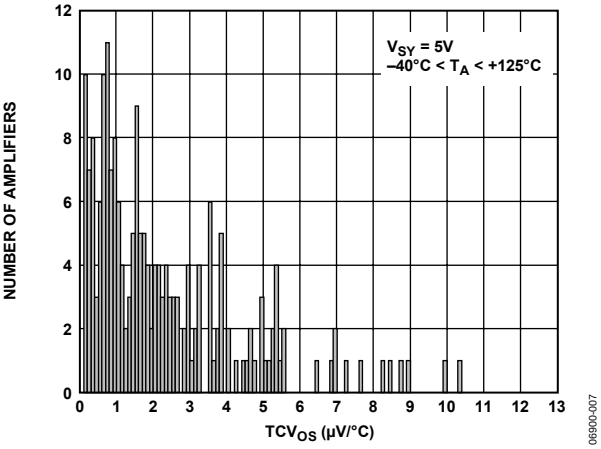


Figure 6. Offset Voltage Drift Distribution

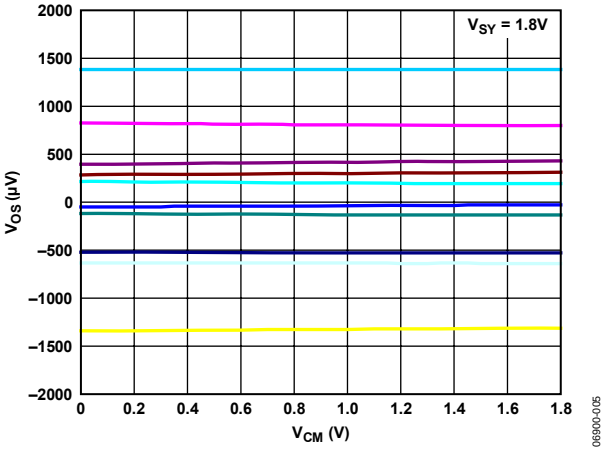


Figure 4. Input Offset Voltage vs. Input Common-Mode Voltage

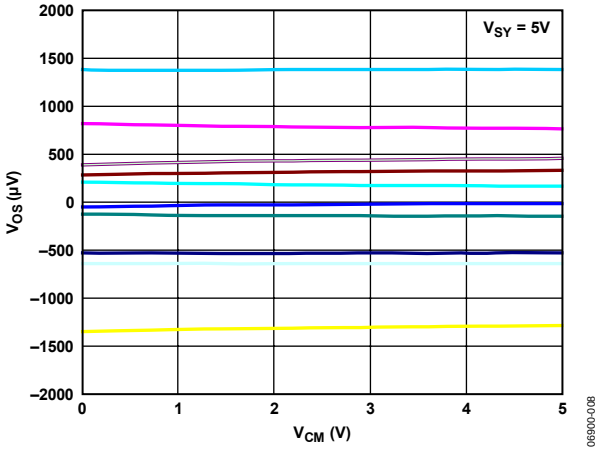


Figure 7. Input Offset Voltage vs. Input Common-Mode Voltage

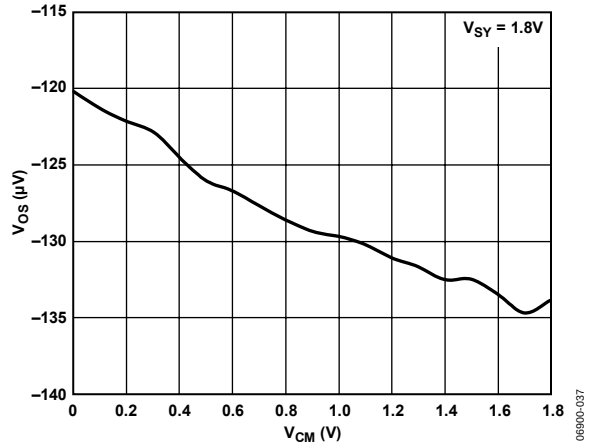


Figure 8. Δ Input Offset Voltage vs. Input Common-Mode Voltage

Figure 11. Δ Input Offset Voltage vs. Input Common-Mode Voltage

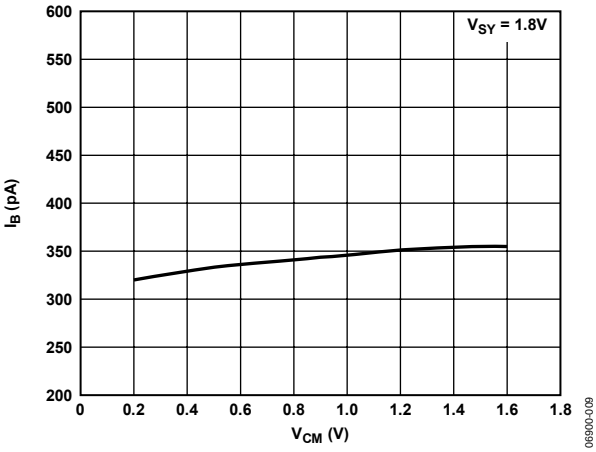


Figure 9. Input Bias Current vs. Common-Mode Voltage at 125°C

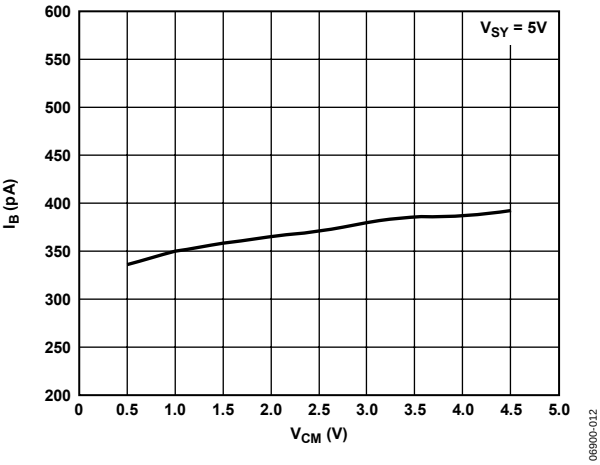


Figure 12. Input Bias Current vs. Common-Mode Voltage at 125°C

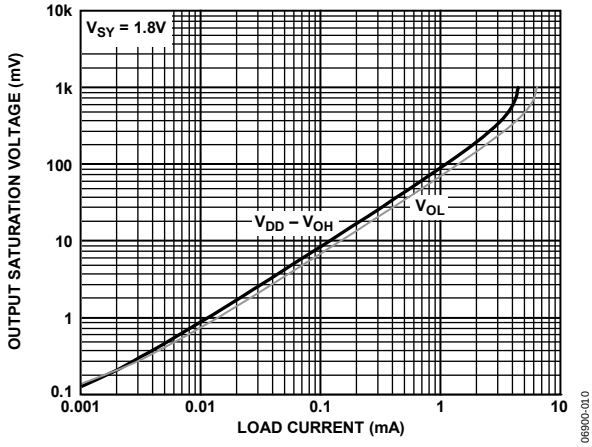


Figure 10. Output Swing Saturation Voltage vs. Load Current

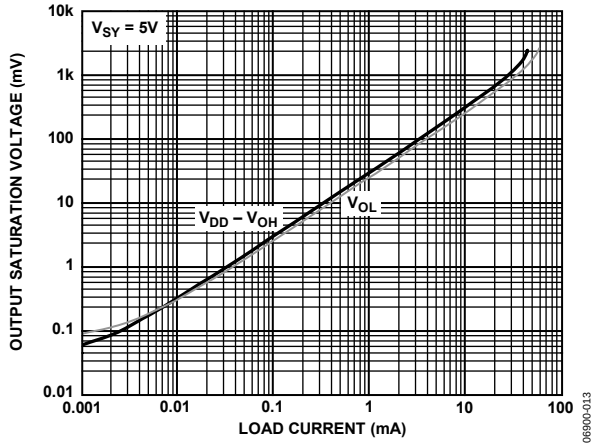


Figure 13. Output Swing Saturation Voltage vs. Load Current

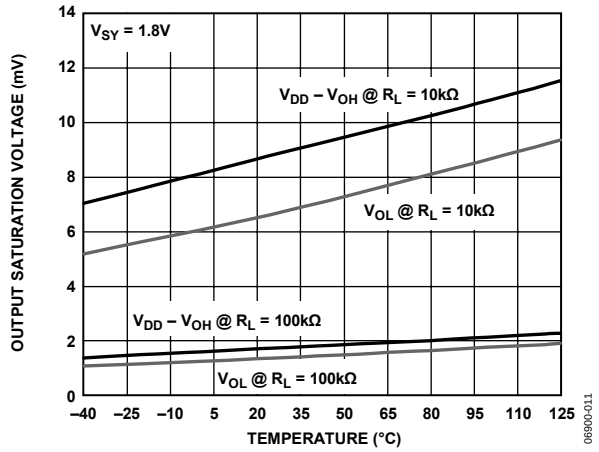


Figure 14. Output Saturation Voltage vs. Temperature

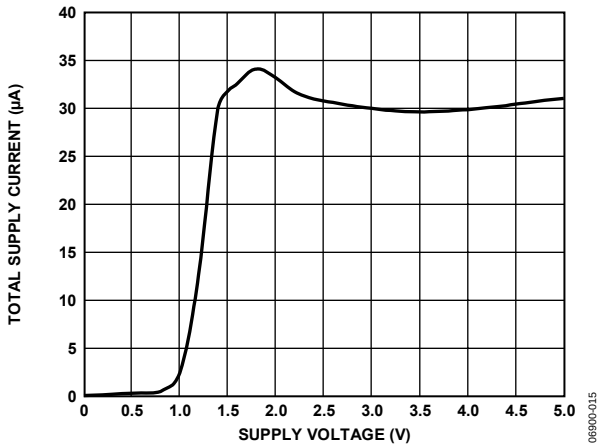


Figure 15. Total Supply Current vs. Supply Voltage

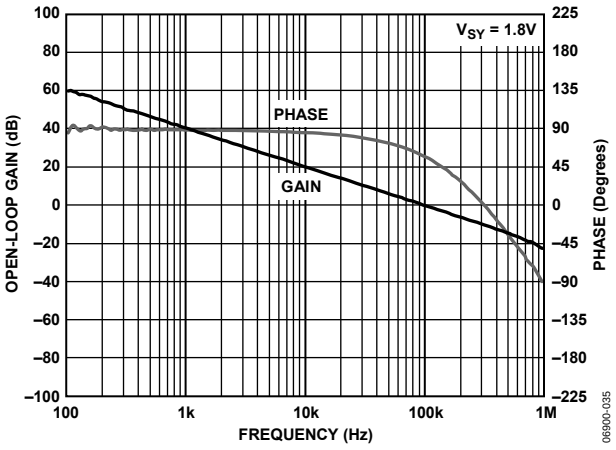


Figure 16. Open-Loop Gain and Phase vs. Frequency

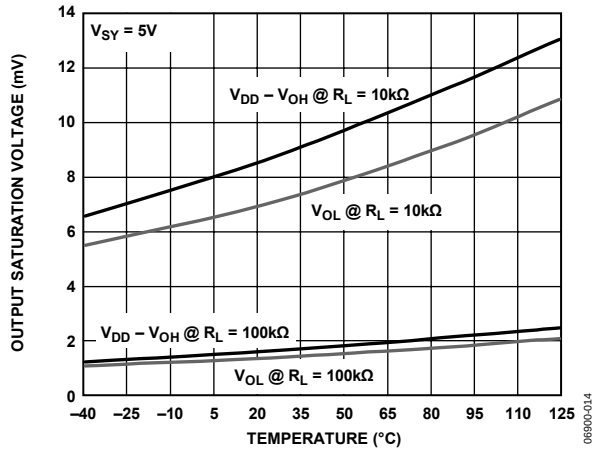


Figure 17. Output Saturation Voltage vs. Temperature

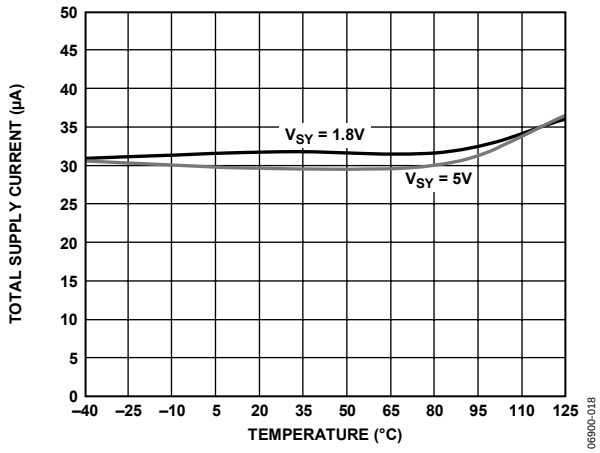


Figure 18. Total Supply Current vs. Temperature

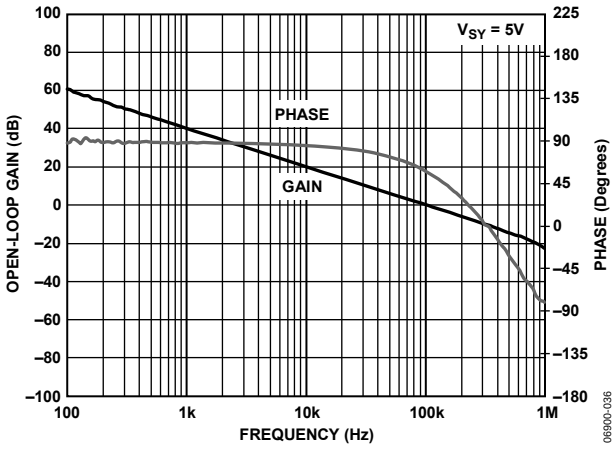


Figure 19. Open-Loop Gain and Phase vs. Frequency

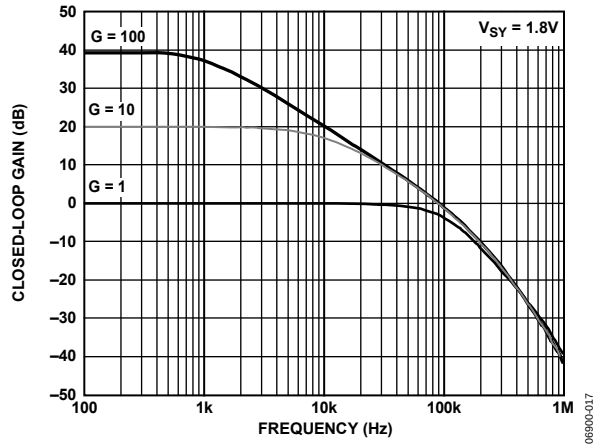


Figure 20. Closed-Loop Gain vs. Frequency

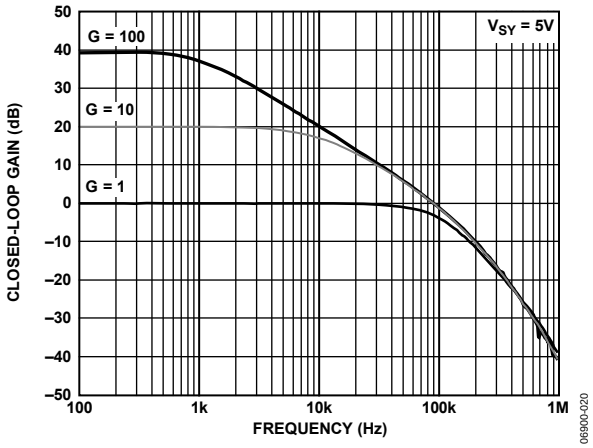


Figure 23. Closed-Loop Gain vs. Frequency

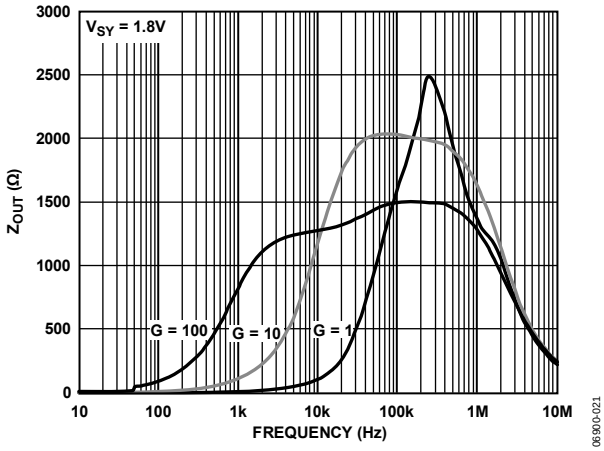


Figure 21. Z_{OUT} vs. Frequency

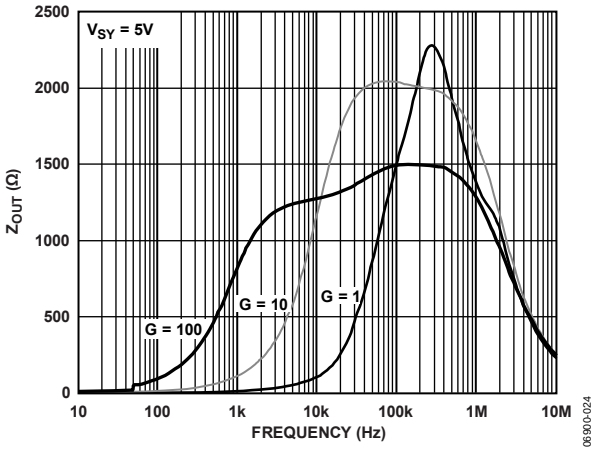


Figure 24. Z_{OUT} vs. Frequency

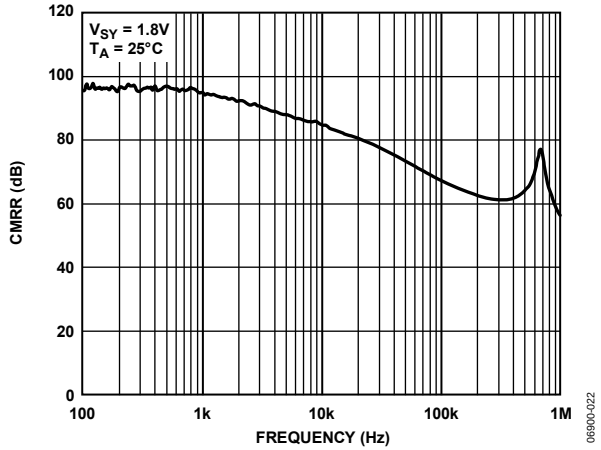


Figure 22. CMRR vs. Frequency

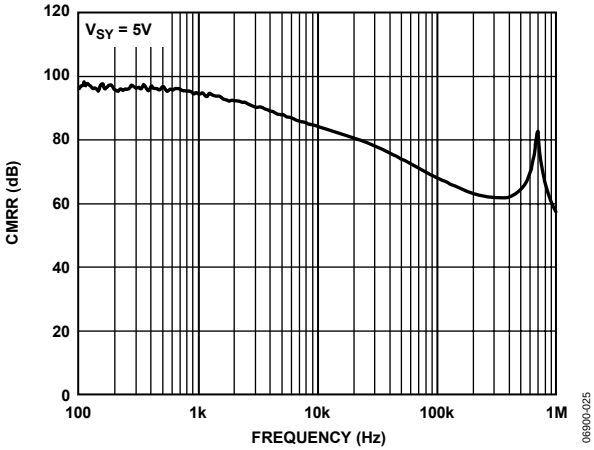


Figure 25. CMRR vs. Frequency

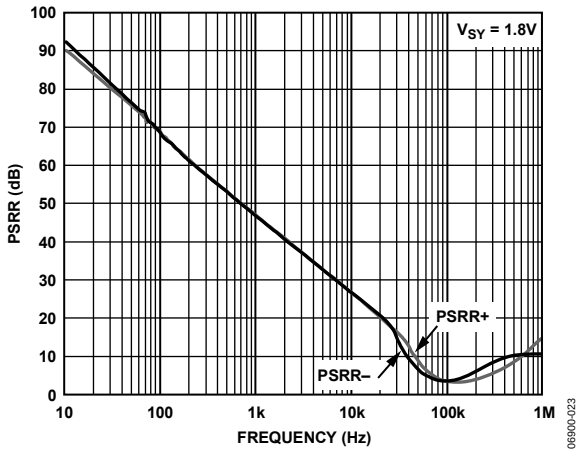


Figure 26. PSRR vs. Frequency

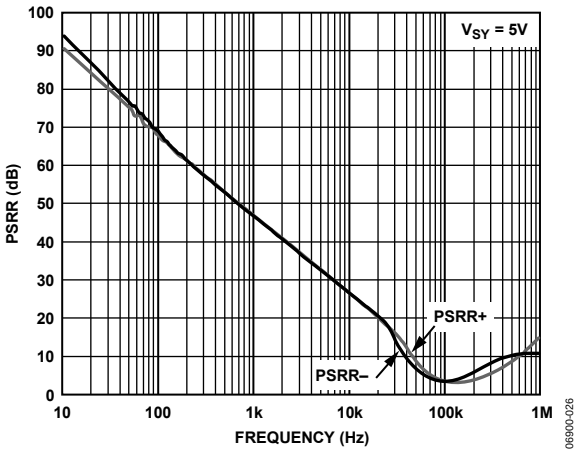


Figure 29. PSRR vs. Frequency

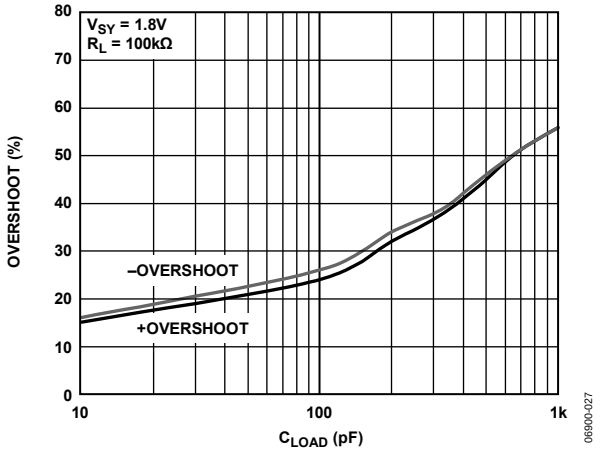


Figure 27. Small Signal Overshoot vs. Load Capacitance

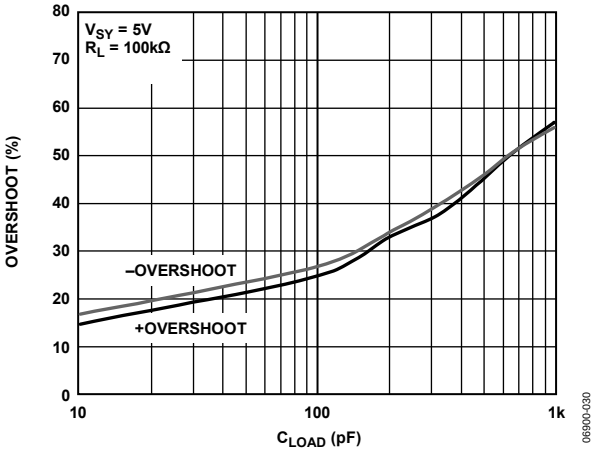


Figure 30. Small Signal Overshoot vs. Load Capacitance

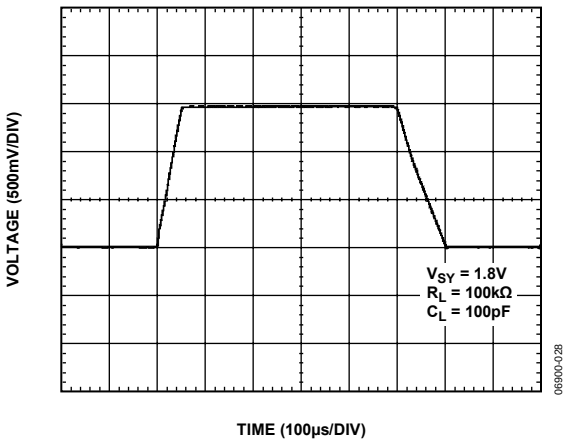


Figure 28. Large Signal Transient Response

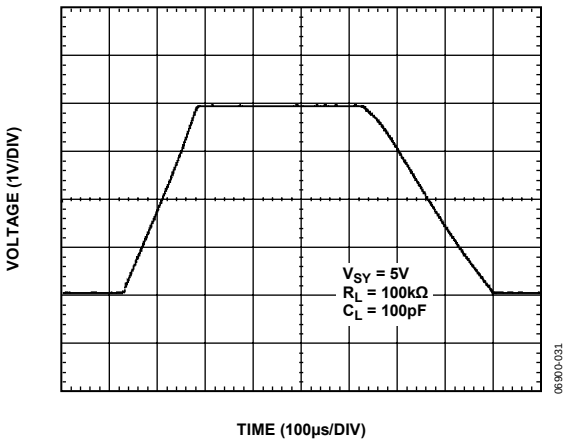


Figure 31. Large Signal Transient Response

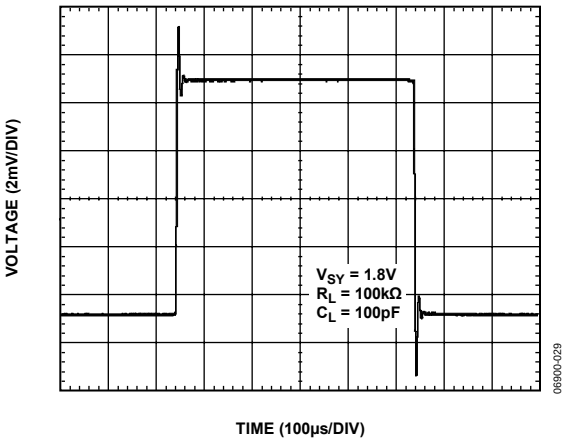


Figure 32. Small Signal Transient Response

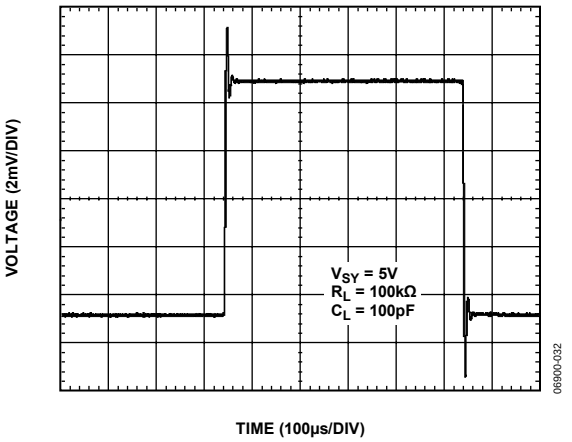


Figure 34. Small Signal Transient Response

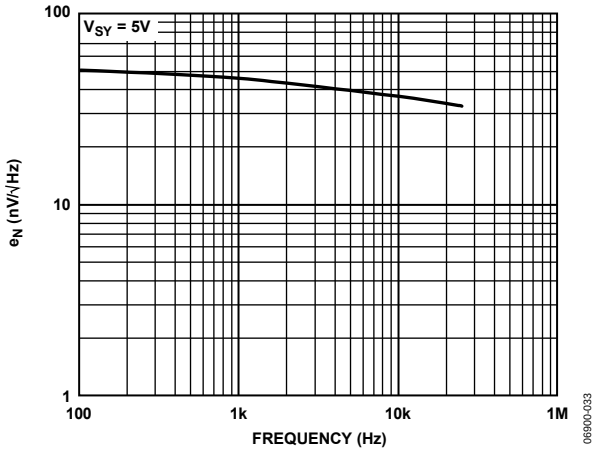


Figure 33. Voltage Noise Density vs. Frequency

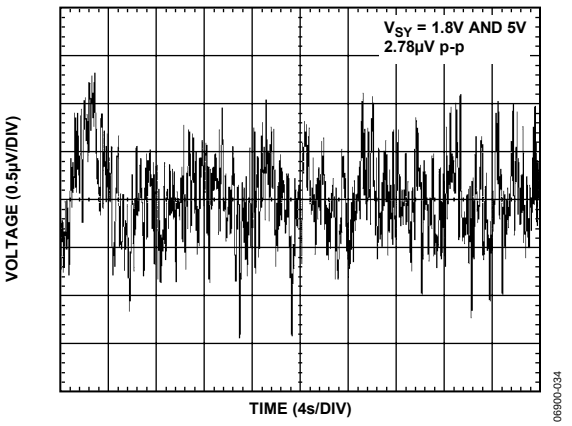
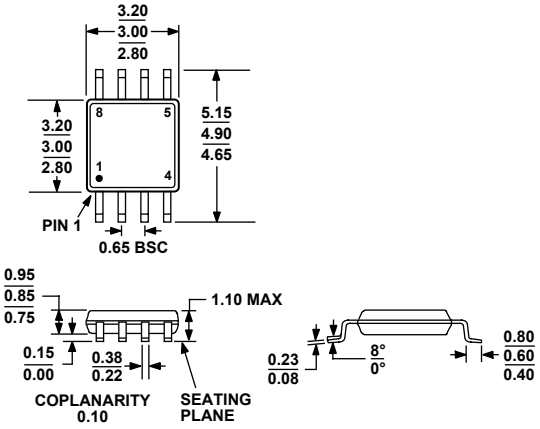


Figure 35. Voltage Noise 0.1 Hz to 10 Hz

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 36. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8506ARMZ-R2[1]	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A1X
AD8506ARMZ-REEL[1]	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A1X

[1] Z = RoHS Compliant Part.

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